

Appl. No. 10/707,175  
Amdt. Dated 08/03/2005  
Reply to Office action of 05/03/05  
**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A method of forming a semiconductor device, comprising:  
providing a semiconductor structure comprising a silicon substrate and a gate structure formed on the silicon substrate, said gate structure further comprising a gate contact and a gate insulator;  
selectively forming etched-away ~~areas~~ regions in the substrate to expose sides of a channel region under the gate structure;  
disposing a thin, highly-doped layer of a silicidation stop material within the etched-away ~~areas~~ regions, the silicidation stop material partially filling the etched-away regions and forming silicidation-stop extensions;  
disposing a silicon fill layer within the etched-away ~~areas~~ regions over the silicidation stop material ~~[[to]]~~; and  
performing silicidation to form silicide in the silicon fill layer, thereby forming source/drain silicide regions;  
wherein the silicon fill layer fills the etched away regions over the thin silicidation-stop extensions, thereby interposing the thin silicidation-stop extensions between the silicon fill layer and the channel region and between the silicon fill layer and the substrate; and  
wherein the silicidation-stop extensions are thin as compared with the silicon fill.
2. (currently amended) A method according to claim 1, wherein the silicidation step is performed at a temperature above a silicidation threshold temperature for the silicide in silicon, but below a silicidation threshold temperature for ~~[[the]]~~ silicide in the silicidation stop material.
3. (currently amended) A method according to claim 2, wherein the silicidation stop material ~~[[is]]~~ comprises SiGe.

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4. (currently amended) A method according to claim 3, wherein the silicide comprises  $\text{CoSi}_2$  (cobalt silicide).
5. (original) A method according to claim 4, wherein the silicidation step is performed at a temperature above a silicidation threshold temperature  $\text{CoSi}_2$  forming in silicon (Si) and below a silicidation threshold temperature for  $\text{CoSi}_2$  formation in SiGe.
6. (original) A method according to claim 4, wherein the silicidation step is performed at a temperature above  $640^\circ\text{C}$  and below  $780^\circ\text{C}$ .
7. (original) A method according to claim 1, wherein the silicidation stop material is in-situ doped.
8. (original) A method according to claim 1, wherein the thickness of silicidation-stop extensions is less than 50% of the thickness of the silicide lateral extensions.
9. (original) A method according to claim 8, wherein the thickness of the silicidation-stop extensions is greater than a minimum thickness defined by the depletion thickness for an active dopant concentration in the silicidation stop material.
10. (original) A method according to claim 9, wherein the active dopant concentration is greater than  $10^{19}$  atoms/cm<sup>3</sup>.
11. (original) A method according to claim 9, wherein the minimum thickness is  $10\text{\AA}$ .
12. (currently amended) A method according to claim 1, wherein the semiconductor structure comprises an inchoate n-channel MOSFET.
13. (currently amended) A method according to claim 1, wherein the semiconductor structure comprises an inchoate p-channel MOSFET.

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14. (currently amended) A method according to claim 1, wherein the semiconductor structure comprises part of an inchoate CMOS device.

Cancel claims 15-25.

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26. (new) A method according to claim 1, wherein the highly-doped layer of the silicidation stop material is formed using an epitaxial growth process.

27. (new) A method according to claim 1, wherein the silicon fill is disposed by a selective Si epi process.

28. (new) A method according to claim 1, wherein the silicidation-stop extensions have a thickness of 10-100Å, and the silicon fill layer has a thickness of approximately 300Å.

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